CHAPTER 31

Configuring POS on the ML-MR-10 Card

This chapter describes advanced packet-over-SONET/SDH (POS) interface configuration for the ML-MR-10 card. Basic POS interface configuration is included in Chapter 6, "Configuring Interfaces." For more information about the Cisco IOS commands used in this chapter, refer to the *Cisco IOS Command Reference* publication. POS operation on ONS Ethernet cards, including the ML-MR-10 card, is described in Chapter 9, "POS on ONS Ethernet Cards."

This chapter contains the following major sections:

POS on the ML-MR-10 Card

Ethernet and IP data packets need to be framed and encapsulated into SONET/SDH frames for transport across the SONET/SDH network. This framing and encapsulation process is known as POS and is done in the ML-MR-10 card. Chapter 9, "POS on ONS Ethernet Cards," explains POS in greater detail.

The ML-MR-10 card takes the standard Ethernet ports on the front of the card and the virtual POS ports and includes them all as switch ports. Under Cisco IOS, the POS port is an interface similar to the other Ethernet interfaces on the ML-MR-10 card. It is usually used as a trunk port. Many standard Cisco IOS features, such as IEEE 802.1 Q VLAN configuration, are configured on the POS interface in the same manner as on a standard Ethernet interface. Other features and configurations are done strictly on the POS interface. The configuration of features limited to POS ports is shown in this chapter.

Note CTC and TL1 displays 26 POS interfaces. However, in Cisco IOS, 18 POS interfaces are available by default.The number of POS interfaces available in Cisco IOS can be modified using the **platform interface-count pos <18-26>** command.

Cisco IOS Commands for POS Ports Configuration

The Cisco IOS commands for modifying POS port configuration and to view the POS ports that are currently available on the ML-MR-10 card are:

- **platform interface-count pos <18-26>** - Modifies the POS port count between 18 and 26. The default number of POS ports is 18. See Example 31-3 on page 31-10.
- **show platform interface-count** - Displays the available POS interfaces. See Example 31-4 on page 31-10.

In an ML-MR-10 card, the default number of POS ports is 18 and the default number of port-channels is 10. The number of POS ports is dependant on the number of port-channel interfaces. The total number of POS ports and port-channels are limited to 28. For example, if the number of POS ports is 24, then the number of configurable port-channels becomes 4.

When the **platform interface-count pos <18-26>** command is executed, the port-channel configuration is affected in the following manner:

- The number of port-channels that can be created is limited by the sum of POS ports and port-channel interfaces, which is 28.

  For example, if the number of POS interfaces is configured as 24, then port-channels 1, 2, 3 and 4 can be created. The remaining port-channel interfaces will not be available.

When the **platform interface-count pos <18-26>** command is executed, the POS ports configuration is affected in the following manner:

- POS port interfaces outside the configured range are not visible on the command line interface (CLI). Hence, these interfaces cannot be configured.
- The queue-threshold values for all the configured POS interfaces are set appropriately.

ML-MR-10 SONET and SDH Circuit Sizes

SONET is an American National Standards Institute (ANSI) standard (T1.1051988) for optical digital transmission at hierarchical rates from 51.840 Mbps (STS-1) to 2.488 Gbps (STS-48) and greater. SDH is the international standard for optical digital transmission at hierarchical rates from 155.520 Mbps (STM-1) to 2.488 Gbps (STM-16) and greater.

Both SONET and SDH are based on a structure that has a basic frame and speed. The frame format used by SONET is the synchronous transport signal (STS), with STS-1 being the base level signal at 51.84 Mbps. A STS-1 frame can be carried in an OC-1 signal. The frame format used by SDH is the synchronous transport module (STM), with STM-1 being the base level signal at 155.52 Mbps. A STM-1 frame can be carried in an OC-3 signal.

Both SONET and SDH have a hierarchy of signaling speeds. Multiple lower level signals can be multiplexed together to form higher level signals. For example, three STS-1 signals can be multiplexed together to form a STS-3 signal, and four STM-1 signals can be multiplexed together to form a STM-4 signal.

SONET circuit sizes are defined as STS-*n,* where *n* is a multiple of 51.84 Mbps and *n* is equal to or greater than 1. SDH circuit sizes are defined as STM-*n*, where *n* is a multiple of 155.52 Mbps and *n* is equal to or greater than 0. Table 31-1 shows STS and STM line rate equivalents.

Table 31-1 SONET STS Circuit Capacity in Line Rate Mbps

SONET Circuit Size	SDH Circuit Size	Line Rate in Mbps
STS-1 (OC-1)	VC-3[1]	52 Mbps
STS-3c (OC-3)	STM-1 (VC4)	156 Mbps
STS-6c (OC-6)	STM-2 (VC4-2c)	311 Mbps
STS-9c (OC-9)	STM-3 (VC4-3c)	466 Mbps
STS-12c (OC-12)	STM-4 (VC4-4c)	622 Mbps
STS-24c (OC-24)	STM-8 (VC4-8c)	1244 Mbps (1.24 Gbps)

Table 31-1 SONET STS Circuit Capacity in Line Rate Mbps

SONET Circuit Size	SDH Circuit Size	Line Rate in Mbps
STS-48c (OC-48)	STM-16 (VC4-16c)	2480Mbps (2.42 Gbps)
STS-192c (OC-192)	STM-64 (VC4-64c)	9920Mbps (9.68 Gbps)

1. VC-3 circuit support requires an XC-VT card to be installed.

For step-by-step instructions on configuring an ML-MR-10 card SONET STS circuit, refer to the "Create Circuits and VT Tunnels" chapter of the *Cisco ONS 15454 Procedure Guide*. For step-by-step instructions on configuring an ML-MR-10 card SDH STM circuit, refer to the "Create Circuits and Tunnels" chapter of the *Cisco ONS 15454 SDH Procedure Guide*.

VCAT

VCAT significantly improves the efficiency of data transport over SONET/SDH by grouping the synchronous payload envelopes (SPEs) of SONET/SDH frames in a nonconsecutive manner into VCAT groups. VCAT group circuit bandwidth is divided into smaller circuits called VCAT members. The individual members act as independent circuits.

Intermediate nodes treat the VCAT members as normal circuits that are independently routed and protected by the SONET/SDH network. At the terminating nodes, these member circuits are multiplexed into a contiguous stream of data. VCAT avoids the SONET/SDH bandwidth fragmentation problem and allows finer granularity for provisioning of bandwidth services.

The ML-MR-10 card VCAT circuits can be routed over a common or a split fiber. These circuits must be both bidirectional and symmetric. The ML-MR-10 card supports upto 26 VT1.5 VCAT groups, with each group corresponding to one of the POS ports. A VCAT circuit originating from an ML-MR-10 card must terminate either on another ML-MR-10 card or a CE-Series card. Table 31-2 shows supported VCAT circuit sizes for the ML-MR-10 card.

Caution Packet losses might occur when an optical fiber is reinserted or when a defect is cleared on members of the HW-LCAS split fiber routed circuits.

Table 31-2 VCAT Circuit Sizes Supported by ML-MR-10 Card

SONET VCAT Circuit Size	SDH VCAT Circuit Size
STS-1-*n*v (1 <=*n* <= 191)	VC3-*n*v (1 <=*n* <= 191)
STS-3c-*n*v (1 <=*n* <= 32)	VC4-*n*v (1 <=*n* <= 32)
VT1.5-*n*v (1 <=*n* <= 63)	VC12-*n*v (1 <=*n* <= 63)

For step-by-step instructions on configuring an ML-MR-10 card SONET VCAT circuit, refer to the "Create Circuits and VT Tunnels" chapter of the *Cisco ONS 15454 Procedure Guide*. For step-by-step instructions on configuring an ML-MR-10 card SDH VCAT circuit, refer to the "Create Circuits and Tunnels" chapter of the *Cisco ONS 15454 SDH Procedure Guide*. For more general information on VCAT circuits, refer to the "Circuits and Tunnels" chapter of the *Cisco ONS 15454 Reference Manual* or the *Cisco ONS 15454 SDH Reference Manual*.

Note ML-Series card POS interfaces normally send an alarm for signal label mismatch failure in the ONS 15454 STS path overhead (PDI-P) to the far end when the POS link goes down or when RPR wraps. ML-Series card POS interfaces do not send PDI-P to the far-end when PDI-P is detected, when a remote defection indication alarm (RDI-P) is being sent to the far end, or when the only defects detected are generic framing procedure (GFP)-loss of frame delineation (LFD), GFP client signal fail (CSF), virtual concatenation (VCAT)-loss of multiframe (LOM), or VCAT-loss of sequence (SQM).

Note For nodes not connected by DCC (open ended nodes), VCAT must be configured through TL1.

On the ML-MR-10 card, members of a HW-LCAS circuit must be moved to the OOS,OOG (locked, outOfGroup) state before:

- Creating or deleting HW-LCAS circuits.
- Adding or deleting HW-LCAS circuit members.
- Changing the state to OOS,DSBLD.
- Changing the state from OOS,DSBLD to any other state.

A traffic hit is seen under the following conditions:

- A hard reset of the card containing the trunk port
- Trunk port moved to OOS,DSBLD(locked,disabled) state
- Trunk fiber pull
- Deletion of members of the HW-LCAS circuit in IG (In Group) state

Note ML-MR-10 cards display symmetric bandwidth behavior when an AIS, UNEQ, LOP, SF, SD, PLM, ENCAP, OOF, or PDI alarm is raised at the near-end member of the HW-LCAS circuit. The LCAS-SINK-DNU alarm and the RDI condition are raised at the far-end member of the circuit. The LCAS-SINK-DNU alarm changes the member state to outOfGroup (OOG) and hence, the traffic goes down in both directions. For more information about alarms, refer to the “Alarm Troubleshooting” chapter in the *Cisco ONS 15454 Troubleshooting Guide* or the *Cisco ONS 15454 SDH Troubleshooting Guide*.

VCAT Circuit Provisioning Time Slot Limitations

The CTC provides different time slots for creating or provision the VCAT circuits for SONET and SDH alarms on the ML-MR-10 card.The time slots vary for different circuits depending on wether the data card present in a high speed slot or low speed slot.

Table 31-3 displays the time slots available for a particular circuit in a particular slot type (high speed or low speed) for SONET alarm.

Table 31-3 VCAT Circuit Provisioning Time Slot Limitations (SONET) on ML-MR-10 Card

Card Mode	Circuit Type	Time Slot Limitation	No. of Members per Circuit
STS-192	STS3c-*n*v	STS-25 is not available. All others available.	63
STS-192	STS1-*n*v	STS-26 is not available. All others available.	191
STS-192	VT1.5-*n*v	Only STS-1,4,49,52,97,100,145,148 are available. All others not available.(Each can hold 24 VT1.5s and hence total is 192)	63
STS-48	STS3c-*n*v	STS-25 is not available. All others available till STS-48.	15
STS-48	STS1-*n*v	STS-26 is not available. All others available till STS-48.	47
STS-48	VT1.5-*n*v	Only STS-7,10,13,16,19,22 are available, All others not available.(Each can hold 24 VT1.5s and hence total is144)	63

Table 31-4 displays the time slots available for a particular circuit in a particular slot type (high speed or low speed) for SDH alarm.

Table 31-4 VCAT Circuit Provisioning Time Slot Limitations (SONET) on ML-MR-10 Card

Card Mode	Circuit Type	Time Slot Limitation	No. of Members per Circuit
STM-64	VC4-*n*v	VC4-9 is not available. All others available.	63
STM-64	VC3-*n*v	VC4-9-2 is not available. All others available.	191
STM-64	VC12-*n*v	Only VC4-1,2,17,18,33,34,49,50 are available. All others not available.(Each can hold 21 VC12s and hence total is 168).	63

Table 31-4 VCAT Circuit Provisioning Time Slot Limitations (SONET) on ML-MR-10 Card

Card Mode	Circuit Type	Time Slot Limitation	No. of Members per Circuit
STM-16	VC4-*n*v	VC4-9 is not available. All others available till VC4-16.	15
STM-16	VC3-*n*v	VC4-1 and VC4-2 completely and VC4-9-2 are not available. All others available till VC4 16.(Each VC4 can hold 3 VC3s).	41
STM-16	VC12-*n*v	Only VC4-3,4,5,6,7,8 are available. All others not available.(Each can hold 21 VC12s and hence total is 126).	63

Note For the CCAT circuits there are no limitations applicable. All time slots are available.

CCAT

Table 31-5 provides the CCAT circuit sizes supported by the ML-MR-10 card for SONET and SDH.

Table 31-5 CCAT Circuit Sizes Supported by ML-MR-10 Card

SONET CCAT Circuit Size	SDH CCAT Circuit Size
STS1	VC3
STS-3c	VC4
STS-6c	VC4-2c
STS-9c	VC4-3c
STS-12c	VC4-4c
STS-24c	VC4-8c
STS-48c	VC4-16c
STS-192c	VC4-64c

SW-LCAS

A link capacity adjustment scheme (LCAS) increases VCAT flexibility by allowing the dynamic reconfiguration of VCAT groups without interrupting the operation of noninvolved members. Software link capacity adjustment scheme (SW-LCAS) is the software implementation of a LCAS-type feature. SW-LCAS differs from LCAS because it is not errorless and uses a different handshaking mechanism.

SW-LCAS on the ONS 15454 SONET and ONS 15454 SDH ML-MR-10 cards allows the automatic addition or removal of a VCAT group member in the event of a failure or recovery on a two-fiber bidirectional line switched ring (BLSR). The protection mechanism software operates based on ML-MR-10 card link events. SW-LCAS allows service providers to configure VCAT member circuits on the ML-MR-10 as protection channel access (PCA) circuits. This PCA traffic is dropped in the event of a protection switch, but is suitable for excess or noncommited traffic and can double the total available bandwidth on the circuit.

For step-by-step instructions on configuring SW-LCAS, refer to the "Create Circuits and VT Tunnels" chapter of the *Cisco ONS 15454 Procedure Guide* or the "Create Circuits and Tunnels" chapter of the *Cisco ONS 15454 SDH Procedure Guide*. For more general information on SW-LCAS, refer to the "Circuits and Tunnels" chapter of the *Cisco ONS 15454 Reference Manual* or the *Cisco ONS 15454 SDH Reference Manual*.

Terminal and Facility Loopback on LCAS Circuits In Split Fibre Routing

The following section lists guidelines to follow when the ML-MR-10 card includes a split fiber routing in a terminal and facility loopback on SW-LCAS circuits:

Note Make sure that you follow the guidelines and tasks listed in the following section. Not doing so will result in traffic going down on members passing through optical spans that do not have loopbacks.

- SW-LCAS circuit members must have J1 path trace set to manual.
- Transmit and receive traces must be unique.
- SW-LCAS circuits on ML-MR-10 must allow our of group (OOG) members on Trace Identifier Mismatch - Path (TIM-P).
- For members on split fiber routes, facility loopback must select the AIS option in CTC.
- Traffic hit is expected when loopback is applied. This is due to asynchronous detection of VCAT defects and TIM-P detection on the other end of the circuit. This is acceptable since loopbacks are intrusive and affect traffic.

However, place members of an HW-LCAS circuit traversing an optical interface under maintenance in OOS,OOG (locked, outOfGroup) state before applying terminal/facility loopbacks.

Framing Mode, Encapsulation, and CRC Support

The ML-MR-10 cards on the Cisco ONS 15454 and Cisco ONS 15454 SDH support only GFP-F framing on both POS and RPR interfaces. On ML-MR POS interfaces, LEX is the only encapsulation supported. On ML-MR POS interfaces, 32-bit CRC is supported and it is always transmitted. The framing mode, encapsulation, and CRC size on source and destination POS ports must match for a POS circuit to function properly. Chapter 9, "POS on ONS Ethernet Cards," explains the framing mechanisms, encapsulations, and cyclic redundancy check (CRC) bit sizes in detail.

Supported encapsulation and CRC sizes for the framing types are detailed in Table 31-6.

Table 31-6 Supported Encapsulation, Framing, and CRC Sizes for ML-MR-10 Cards on ONS 15454 and ONS 15454 SDH

	Encapsulations for GFP-F Framing	CRC Sizes for GFP-F Framing
ML-MR-10	LEX (default)	32-bit (default)

Note ML-MR-10 card POS interfaces normally send PDI-P to the far-end when the POS link goes down or RPR wraps. ML-MR-10 card POS interfaces do not send PDI-P to the far-end when PDI-P is detected, when RDI-P is being sent to the far-end, or when the only defects detected are GFP LFD, GFP CSF, VCAT LOM, or VCAT SQM. Also, GFP-FCS is always transmitted on the ML-MR-10 card.

Note The HDLC encapsulation can be configured on POS. However, the circuit does not come up and the configuration should be blocked. For information on Framing and Encapsulation on the ML-Series cards, see Framing Mode, Encapsulation, and CRC Support, page 8-4 in Chapter 8, “Configuring POS”.

Monitoring and Verifying POS

The **show controller pos** *[0 |* command (Example 31-1) outputs the receive and transmit values and the C2 value. Thus, changing the value on the local end does not change the value in the **show controller** command output.

Example 31-1 show controller pos [0 | Command with a VCAT Circuit

```
ML-MR # show controllers pos0
Interface POS0
Hardware is Packet Over SONET
Framing Mode: GFP

Path Trace Info.
Channel 48
Received String Format : 64 Byte
Transmit String Format : 16 Byte
Provisioned Trace Mode : off
Prov'd : false TIU-P : FALSE TIM-P : FALSE
State : w4xcon MatchCnt: 0 MisMatchCnt: 0
Rec Flag : false Exp Flag : false Xmt Enab : true

0 total input counters 0 total crc

0 total output bytes

Carrier delay is 200 msec


Concatenation: VCAT
Alarms reportable to CLI: AIS-V LOP-V UNEQ-V TIM-V PLM-V ENCAP-MISMATCH RDI-V PDI-V SF-V
SD-V OOU_TPT-VT LOM-VT SQM-VT
Link state change defects: AIS LOP UNEQ PLM ENCAP RDI PDI LOA LOM SQM GFP_LFD GFP_CSF
Link state change time : 200 (msec)
*************** GFP ***************
Active Alarms : None
Demoted Alarms: None
LDF = 0 CSF = 0
***************** VCG ******************
ESM State:unlocked
Number of Planned/Working Members: 1 / 1
LCAS Type:NO LCAS
Physical Channel Number: 4
Active Alarms: None

************ Member 0 ***************
Member Type: VC-12
Member State: MBR IU
Circuit ESM State: unlocked
VT index 168, STS No. 147
Active Alarms: None
Extended signal label 0D
VT BER Thresholds:
SFBER = 1e-4, SDBER = 1e-6

Defect Processing Mode: IMMEDIATE
PDI Holdoff Time: 100 (msec)

0 total input counters 0 total crc

435960 total output bytes

Carrier delay is 200 msec
```

Example 31-2 show controller pos [0 | 1] Command with a CCAT Circuit

```
ML-MR#show controllers pos2
Interface POS2
Hardware is Packet Over SONET
```

```
Framing Mode: GFP
Concatenation: CCAT
Alarms reportable to CLI: AIS-P LOP-P UNEQ-P TIM-P PLM-P ENCAP-MISMATCH RDI-P PDI-P SF-P
SD-P
Link state change defects: AIS LOP UNEQ PLM ENCAP RDI PDI GFP_LFD GFP_CSF
Link state change time : 200 (msec)

*************** GFP ***************
Active Alarms : None
Demoted Alarms: None
LDF = 0 CSF = 0
*************** Path ***************
Circuit Type: VC4-16C
Physical Channel Number: 6
Circuit ESM State: unlocked, automaticInservice
STS Index 48
Active Alarms: None

C2 1B

B3 BER thresholds:
SFBER = 1e-5, SDBER = 1e-7
```

Example 31-3 platform interface-count pos <18-26>

```
Node_51#conf t
Node_51(config)#platform interface-count pos 26
Number of port-channel interfaces allowed is changed to: 2
Node_51(config)#exit
```

Example 31-4 show platform interface-count

```
Node_51#show platform interface-count
Max number of POS interfaces: 26
        (POS0 through POS25)
Max number of port-channel interfaces: 2
        (port-channel1 through port-channel2)
```