# IOS Catalyst 6500/6000 Resets with Error "System returned to ROM by power-on (SP by abort)"

Document ID: 50560

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## Introduction

A Cisco Catalyst 6500/6000 that runs Cisco IOS® Software can appear to reload with this reset reason:

```
System returned to ROM by power-on (SP by abort)
```

A mismatch of the configuration register settings can cause this type of reload. Specifically, you can set the Supervisor Engine Switch Processor (SP) configuration register to a value that does not "ignore break", while the Multilayer Switch Feature Card (MSFC) Route Processor (RP) configuration register is a proper value that does "ignore break". For example, you can set the Supervisor Engine SP to 0x2 and the MSFC RP to 0x2102.

# **Prerequisites**

## Requirements

Readers of this document should have knowledge of these topics:

• The difference between Catalyst OS (CatOS) and Cisco IOS System Software

Refer to the "Difference Between CatOS and Cisco IOS System Software" section of the document System Software Conversion from CatOS to Cisco IOS for Catalyst 6500/6000 Switches

• CatOS and Cisco IOS Software configuration registers

Refer to these documents:

- ♦ Modifying the Switch Boot Configuration
- ◆ "Configuring the Software Configuration Register" section of the document Configuring the Switch for the First Time

## **Components Used**

This document is restricted to Catalyst 6500/6000 switches that run Cisco IOS Software.

The information in this document was created from the devices in a specific lab environment. All of the devices used in this document started with a cleared (default) configuration. If your network is live, make sure that you understand the potential impact of any command.

#### **Conventions**

For more information on document conventions, refer to the Cisco Technical Tips Conventions.

# **Background Information**

A Catalyst 6500/6000 that runs in Cisco IOS Software mode can have different configuration registers for the SP and RP. The running and startup configurations are in synchronization between the SP and RP while in Cisco IOS Software mode. However, the configuration register is not part of the running or startup configuration. The configuration register writes to NVRAM at configuration.

Configuration register settings that do not "disable break", such as 0x2, cause a Cisco IOS device to enter ROM monitor (ROMmon) diagnostic mode when the console receives a break signal. A break signal generates if you press the appropriate break key sequence in the terminal emulator software, or via other means. An example break key sequence is Ctrl-Break in HyperTerminal. Under very specific hardware (PC) configurations, a break sequence forwards to the console without the press of any keys within a terminal emulator. A hardware malfunction or interoperability issue typically causes this occurrence. The causes include proprietary serial port pinouts and radio frequency (RF) noise.

When in CatOS mode, Supervisor Engine SPs commonly have the configuration register 0x2. The reason for this configuration is that "disable break" is not an option in CatOS; when CatOS detects a break signal, CatOS does not enter ROMmon with a configuration register of 0x2.

This output is from a Catalyst 6500 that runs CatOS:

```
6500_CATOS (enable) show boot
BOOT variable = bootflash:,1;
CONFIG_FILE variable = slot0:switch.cfg

Configuration register is 0x2
ignore-config: disabled
auto-config: non-recurring, overwrite, sync disabled
console baud: 9600
boot: image specified by the boot system commands
```

Cisco IOS routers, which include MSFCs, typically have the appropriate configuration registers of 0x102 or 0x2102. The 0x2102 configuration does "disable break".

```
MSFC# show bootvar
BOOT variable = bootflash:c6msfc2-psv-mz.121-13.E14,1
CONFIG_FILE variable =
BOOTLDR variable =
Configuration register is 0x2102
```

Consider the conversion to Cisco IOS Software of a Catalyst 6500 system for which you have set the Supervisor Engine SP configuration register to 0x2 and the MSFC RP configuration register to 0x2102. At conversion, the configuration registers remain the same until the reconfiguration of the configuration register when the conversion is complete. In this state, if the console receives a break signal, the system appears to crash as it enters ROMmon. The system exhibits the symptoms that the Introduction of this document describes.

This is an example of a mismatch of configuration registers in a Catalyst 6500/6000 in Cisco IOS Software mode:

```
6500_IOS# show bootvar
BOOT variable = slot0:c6sup12-ps-mz.121-13.E14,1
CONFIG_FILE variable =
BOOTLDR variable =
Configuration register is 0x2102

6500_IOS# remote command switch show bootvar

6500_IOS-sp#
BOOT variable = slot0:c6sup12-ps-mz.121-13.E14,1
CONFIG_FILE variable =
BOOTLDR variable =
Configuration register is 0x2
```

# **Problem**

A Catalyst 6500/6000 with an SP configuration register that allows break, for example 0x2, and that receives a console break signal enters ROMmon diagnostic mode. The system appears to crash.

This example switch output indicates that the switch entered ROMmon diagnostic mode from a switch processor console break signal:

**Note:** The RP configuration register is 0x2102.

```
6500_IOS# show version
Cisco Internetwork Operating System Software
IOS (tm) c6sup2_rp Software (c6sup2_rp-PS-M), Version 12.1(13)E14, EARLY DEPLOYMENT
RELEASE SOFTWARE (fc1)
Technical Support: http://www.cisco.com/techsupport
Copyright (c) 1986-2004 by Cisco Systems, Inc.
Compiled Tue 30-Mar-04 01:56 by pwade
Image text-base: 0x40008C00, data-base: 0x417A6000
ROM: System Bootstrap, Version 12.1(4r)E, RELEASE SOFTWARE (fc1)
BOOTLDR: c6sup2_rp Software (c6sup2_rp-PS-M), Version 12.1(13)E14, EARLY DEPLOYMENT
RELEASE SOFTWARE (fc1)
6500 IOS uptime is 31 minutes
Time since 6500_IOS switched to active is 31 minutes
System returned to ROM by power-on (SP by abort at PC 0x601061A8)
System image file is "slot0:c6sup12-ps-mz.121-13.E14"
cisco Catalyst 6000 (R7000) processor with 227328K/34816K bytes of memory.
Processor board ID SAD053701CF
R7000 CPU at 300Mhz, Implementation 39, Rev 2.1, 256KB L2, 1024KB L3 Cache
Last reset from power-on
X.25 software, Version 3.0.0.
Bridging software.
1 Virtual Ethernet/IEEE 802.3 interface(s)
192 FastEthernet/IEEE 802.3 interface(s)
18 Gigabit Ethernet/IEEE 802.3 interface(s)
381K bytes of non-volatile configuration memory.
16384K bytes of Flash internal SIMM (Sector size 512K).
Configuration register is 0x2102
```

## **Solution**

The solution is to reconfigure the configuration register and reload the system.

Complete these steps:

1. In global configuration mode, issue the **config-register 0x2102** command, and set the configuration register to 0x2102 for both the RP and the SP.

```
6500_IOS# config t
Enter configuration commands, one per line. End with CNTL/Z.
6500_IOS(config)# config-register 0x2102
6500_IOS(config)# end
```

2. To verify the configuration register value at the next reload, issue the **show bootvar** command.

```
6500_IOS# show bootvar
BOOT variable = slot0:c6sup12-ps-mz.121-13.E14,1
CONFIG_FILE variable =
BOOTLDR variable =
Configuration register is 0x2102
```

3. To verify that the configuration register on the SP also changed, issue the **remote command switch show bootvar** command.

```
6500_IOS# remote command switch show bootvar

6500_IOS-sp#
BOOT variable = slot0:c6sup12-ps-mz.121-13.E14,1
CONFIG_FILE variable =
BOOTLDR variable =
Configuration register is 0x2 (will be 0x2102 at next reload)
```

4. Reload the switch for the new SP configuration register setting to take effect.

```
6500_IOS# reload
```

**Note:** You can issue the **copy running–config startup–config** command at this point to save the configuration. However, this step is not necessary because the configuration register setting is not part of the startup or running configuration.

## **Related Information**

- LAN Product Support Pages
- LAN Switching Support Page
- Technical Support Cisco Systems

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Updated: Sep 01, 2005