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Cisco Nexus V5P FPGA Application SmartNIC

Contents

High-density network application card

The Cisco Nexus® V5P FPGA Application SmartNIC is an FPGA-based network application card, specifically optimized for low-latency and high-density data center applications.

The Cisco Nexus V5P FPGA Application SmartNIC adapters are equipped with a powerful 16nm Xilinx Virtex UltraScale Plus (VU5P) FPGA with up to 1.3M logic cells, packaged into a compact, production ready, half-height half-length, PCIe 8x form factor.

High-capacity, low-latency memory

An extensive memory hierarchy for complex, memory intensive applications.

The Cisco Nexus V5P FPGA Application SmartNIC includes 36Mbit of block RAM and 133Mbit of UltraRAM on chip for low-latency access. The Cisco Nexus V5P FPGA Application SmartNIC incorporates an additional 18MB of QDR IV SRAM (30ns access latency using Cisco Nexus QDR controller IP1), and 9GB of DDR4 DRAM for high throughput access. The DRAM is accessible via a 72 bit wide bus for maximum performance.

High-bandwidth connectivity

Dual QSFP28 ports provide up to 200Gbps of full duplex connectivity.

The dual QSFP28 cages offer high-speed 2x40GbE or 2x100GbE connectivity. Using QSFP/QSFP28 breakout cables expands the connectivity to 8x10GbE/25GbE connections. This high-density connectivity enables a range of high-performance, directly connected network applications, bypassing the need for traditional switching and multiplexing requirements.

Extensive IP library

Cisco is a specialist in low-latency, high-performance FPGA IP cores.

We provide to you the same high-speed, low-latency IP blocks used in our industry-leading products, including:

- 10GbE PCS/MAC with ultra-low latency performance.
- Low-latency, high-throughput PCIe (Gen 3) DMA engine.
- Timing, signaling, and register interfaces, including I2C
- Packet field extractor and frame multiplexer (with source code)
- Asynchronous FIFO and CDC modules (with source code)

Several example designs are also provided to help get design work started and completed quickly.

Integrated software library

A standard Linux driver as well as transparent TCP and UDP acceleration and low-level packet access.

Like all SmartNICs, the Cisco Nexus V5P FPGA Application SmartNIC functions out of the box as a high-performance network adapter. The entire SmartNIC software library is available including the sockets application acceleration system and the libexanic direct userspace accesses API. Libexanic provides easy support for low-latency packet TX/RX, managing the FPGA state (through register access), and low-latency TCP/UDP-delegated sending operations for hybrid hardware/software applications. The Cisco Nexus V5P FPGA Application SmartNIC also supports fast and easy firmware updates (without requiring reboots), and vital statistics monitoring (temperatures, voltages, light levels, fans, etc.).
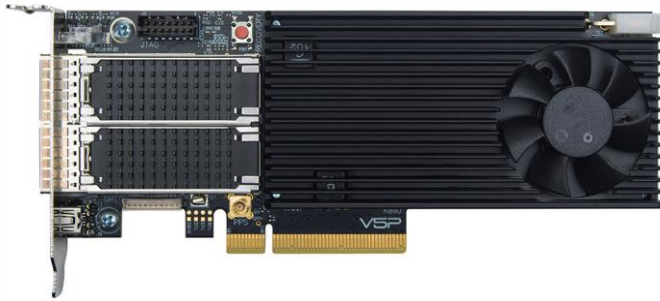

Figure 1.
Cisco Nexus V5P FPGA Application SmartNIC

Hardware

16nm Xilinx Virtex UltraScale+ FPGA:

- XCVU5P-2 (A2104)
- 1.3M System Logic Cells, 1.2M CLBs
- 36Mb total block RAM
- 133Mb UltraRAM
- 16x 32.75Gb/s transceivers (8 connected to QSFPs, 8 connected to PCIe)

QDR IV SRAM:

- 144MBit
- Dual 36-bit interface, up to 1066MHz
- 30ns read using Cisco IP

DDR4 DRAM:

- 9GByte
- 72-bit interface, up to 2666MHz

Oscillators:

- 161MHz crystal

- 10MHz temperature compensated crystal

- 10MHz – 750Hz programmable (I2C) crystal

Input/output:

- PPS in/out via MCX connector, 3.3V CMOS, selectable 50ohm termination

- 8x 1.8V CMOS GPIO via header

- 2x bi-color port LEDs

- 12V external supply (GPU adapter) for >25W designs

Programming/debugging:

- Software-based PCIe flash programming utility

- Easy access, front panel USB to JTAG port

- JTAG header on board (auto select)

- 1Gbit onboard flash (space for 2x full images)

Performance

PCS/MAC (TX + RX)[2]:

- 6.2ns (min) @ 10Gbps

- 1Gbps/100Mbps also supported

SERDES/PCS/MAC/CDC (TX+RX):

- Packet trigger, 34ns (min)[2]

- Full loopback, 50ns (min)

Software latency (raw frame, ½RTT)[1]:

- 64 bytes – 810ns

- 256 bytes – 1030ns

General

Form factor:

- Low-profile PCI Express Card
- 168x69mm (6.6x2.7in)

Environmental:

- SmartNIC operating temperature: 0 °C to 55 °C
- SmartNIC storage temperature: -40 °C to 70 °C
- FPGA operating temperature: 0 °C to 100 °C
- Operating Relative Humidity: 5% to 90% (non-condensing)
- Storage Relative Humidity: 5% to 95% (non-condensing)

Ports:

- 2x QSFP28
- SMA for PPS in/out
- USB to JTAG

Host interface:

- PCIe x8 Gen 3 @ 8.0 GT/s per lane

Data rates:[3]

- 100GbE, 50GbE, 40GbE, 25GbE, 10GbE, 1GbE, 100M Fast Ethernet

Supported media:

- Fiber (100GBASE-SR4, 100GBASE-LR4, 40GBASE-SR4, 40GBASE-LR4), QSFP/28 Direct Attach breakout

Operating systems:

- Linux x86_64 (all distributions)

Cisco environmental sustainability

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Reference links to information about key environmental sustainability topics (mentioned in the "Environment Sustainability" section of the CSR Report) are provided in the following table:

Sustainability topic	Reference
Information on product material content laws and regulations	Materials
Information on electronic waste laws and regulations, including products, batteries, and packaging	WEEE compliance

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Footnotes

[1] Preliminary results only. Final results to be confirmed.

[2] RX + TX time for PMA + PCS + MAC + CDC performing packet trigger based on first data word (for example, dst MAC).

[3] 25GbE functionality available via firmware upgrade. 40/50/100GbE requires user supplied MAC.