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Balzs Dn <balazs.dan@gmail.com>  
Bharat Mediratta <bharat@menalto.com>  
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Ji Sigursson <joi@google.com>  
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Preston Jackson <preston.a.jackson@gmail.com>  
Rainer Klaffenboeck <rainer.klaffenboeck@dynatrace.com>  
Russ Cox <rsc@google.com>  
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```
=====
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s
```

```
define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:
```

```
    ; First, extend each i32 to i64
```

```
    ; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
```

```
    ; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
```

```
    ; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
```

```
    ; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
```

```
    ; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
```

```
    ; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
```

```
    ; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
```

```
    ; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0
```

```
    ; Next, convert each to double.
```

```
    ; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
```

```
    ; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
```

```
    ; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
```

```
    ; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
```

```
    ; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
```

```
    ; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
```

```
    ; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
```

```
    ; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]
```

```
    ; CHECK: ret
```

```
    %flt = sitofp <16 x i32> %in to <16 x double>
```

```
    %res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0>
```

```
ret <16 x double> %res
}
```

; This one is small enough to satisfy isSimple, but still illegally large.

```
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
```

```
; CHECK-LABEL: test_sitofp_fixed_shortish:
```

```
; CHECK-DAG: scvtf.2d v0, v0
```

```
; CHECK-DAG: scvtf.2d v1, v1
```

```
; CHECK: ret
```

```
%flt = sitofp <4 x i64> %in to <4 x double>
```

```
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
```

```
ret <4 x double> %res
```

```
}
```

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Arne Beer <arne@twobeer.de>

Billy Robert O'Neal III <billy.oneal@gmail.com> <bion@microsoft.com>

Chris Kennelly <ckennelly@google.com> <ckennelly@ckennelly.com>

Christopher Seymour <chris.j.seymour@hotmail.com>

David Coeurjolly <david.coeurjolly@liris.cnrs.fr>

Dominic Hamon <dma@stripsock.com>

Eric Fiselier <eric@efcs.ca>

Eugene Zhuk <eugene.zhuk@gmail.com>

Evgeny Safronov <division494@gmail.com>

Felix Homann <linuxaudio@showlabor.de>

Ismael Jimenez Martinez <ismael.jimenez.martinez@gmail.com>

JianXiong Zhou <zhoujianxiong2@gmail.com>

Jussi Knuutila <jussi.knuutila@gmail.com>

Kaito Udagawa <umireon@gmail.com>

Kai Wolf <kai.wolf@gmail.com>

Lei Xu <eddyxu@gmail.com>  
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```
add_lldb_library(lldbPluginObjectContainerBSDArchive  
ObjectContainerBSDArchive.cpp  
)
```

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; RUN: llc -march=hexagon < %s

; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types

; cause LSR to assume type "void" for the memory type. This would then

; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

```
target triple = "hexagon"
```

```
%struct.0 = type { i8*, i8, %union.anon.0 }
```

```
%union.anon.0 = type { i8* }
```

```
define hidden fastcc void @fred() unnamed_addr #0 {
```

```
entry:
```

```
br i1 undef, label %while.end, label %while.body.lr.ph
```

```
while.body.lr.ph:                                ; preds = %entry
```

```
br label %while.body
```

```
while.body:                                       ; preds = %exit.2, %while.body.lr.ph
```

```
%lshr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
```

```
switch i32 undef, label %exit [
```

```
  i32 1, label %sw.bb.i
```

```
  i32 2, label %sw.bb3.i
```

```
]
```

```
sw.bb.i:                                          ; preds = %while.body
```

```
unreachable
```

```
sw.bb3.i:                                         ; preds = %while.body
```

```
unreachable
```

```
exit:                                             ; preds = %while.body
```

```
switch i32 undef, label %exit.2 [
```

```
  i32 1, label %sw.bb.i17
```

```
  i32 2, label %sw.bb3.i20
```

```
]
```

```
sw.bb.i17:                                       ; preds = %exit
```

```
%0 = bitcast %struct.0* %lshr.iv to i32*
```

```
%1 = load i32, i32* %0, align 4
```

```
unreachable
```

```
sw.bb3.i20:                                       ; preds = %exit
```

```
%2 = bitcast %struct.0* %lshr.iv to i8**
```

```
%3 = load i8*, i8** %2, align 4
```

```
unreachable
```

```
exit.2:                                           ; preds = %exit
```

```
%cgep22 = getelementptr %struct.0, %struct.0* %lshr.iv, i32 1
```

```
br label %while.body
```

```
while.end:                                        ; preds = %entry
```

```
ret void
}
```

```
attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
```

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